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(56) Documents Cited
GB 2273224 A GB 2238934 A WO 94/24794 A1

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INT CL^6 H04J 3/26 , H04L 12/18 12/52 12/56 , H04Q 11/04
Online: WPI, INSPEC

(54) Reducing delays and bandwidth requirements in a point-to-multipoint packet communication system

(57) A number of multiplexer units 40, 50 and 62 are connected via a circuit switch 44. When multiplexer A receives an information packet intended for at least two other destinations 50, 62, it elicits the address information and information bits from the information packet. Based on this address information, a communications channel is selected for transmission of the information packet from the first multiplexer unit to the circuit switch. At the circuit switch the information packet is duplicated to provide at least two information packets for transmission on at least two outputs of the circuit switch 48. The at least two information packets are transmitted from the circuit switch to second and third multiplexer units respectively on the at least two outputs. This arrangement reduces the delays incurred if the same packet was repeatedly sent to the different destinations. It also reduces the bandwidth penalties that would be incurred if a "true" multicast approach was adopted whereby each packet would be transmitted to all destinations.

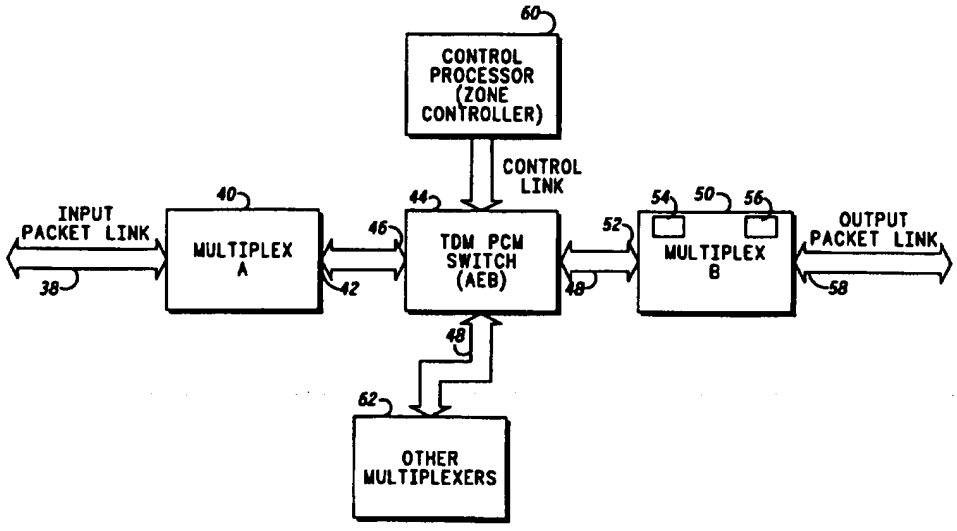

FIG. 2

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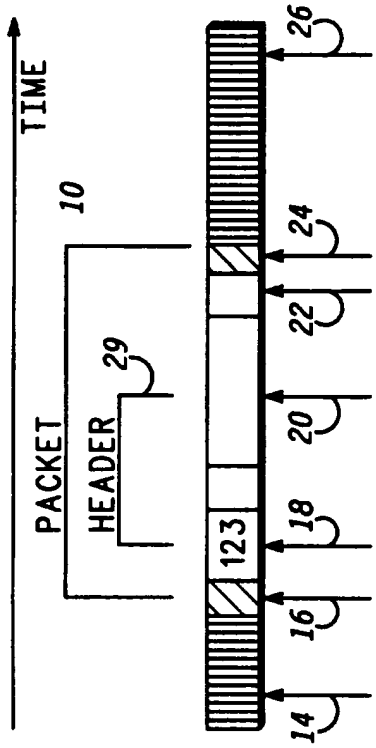


FIG. 1

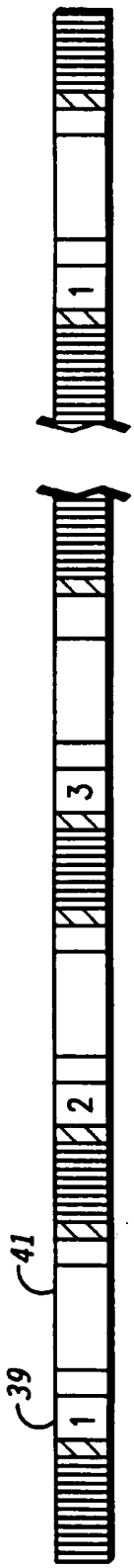
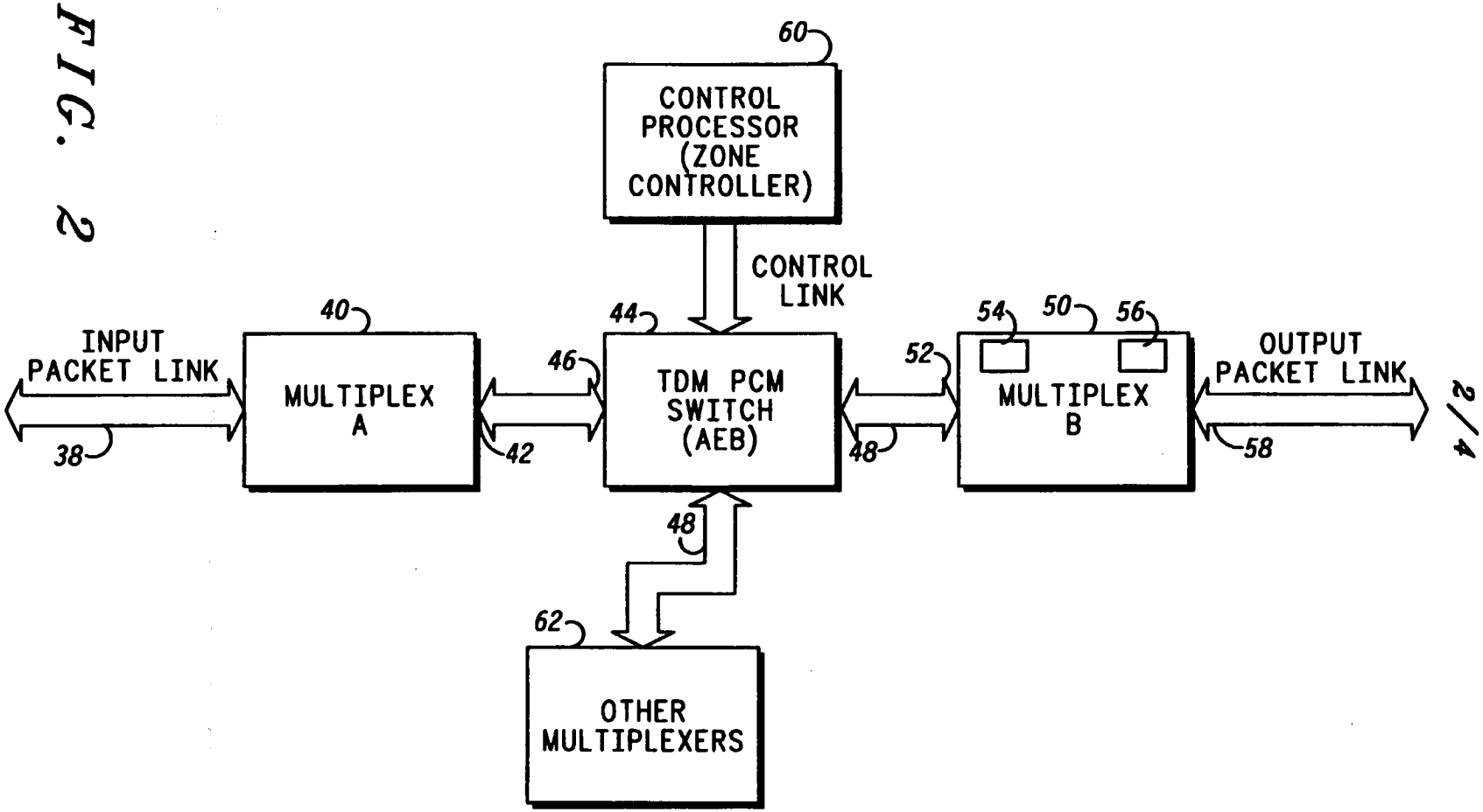


FIG. 3

FIG. 2


60
CONTROL PROCESSOR (ZONE CONTROLLER)
CONTROL LINK
40
44
54
50
56
INPUT PACKET LINK
MULTIPLEX A
46
TDM PCM SWITCH (AEB)
52
MULTIPLEX B
OUTPUT PACKET LINK
38
42
48
58
48
62
OTHER MULTIPLEXERS

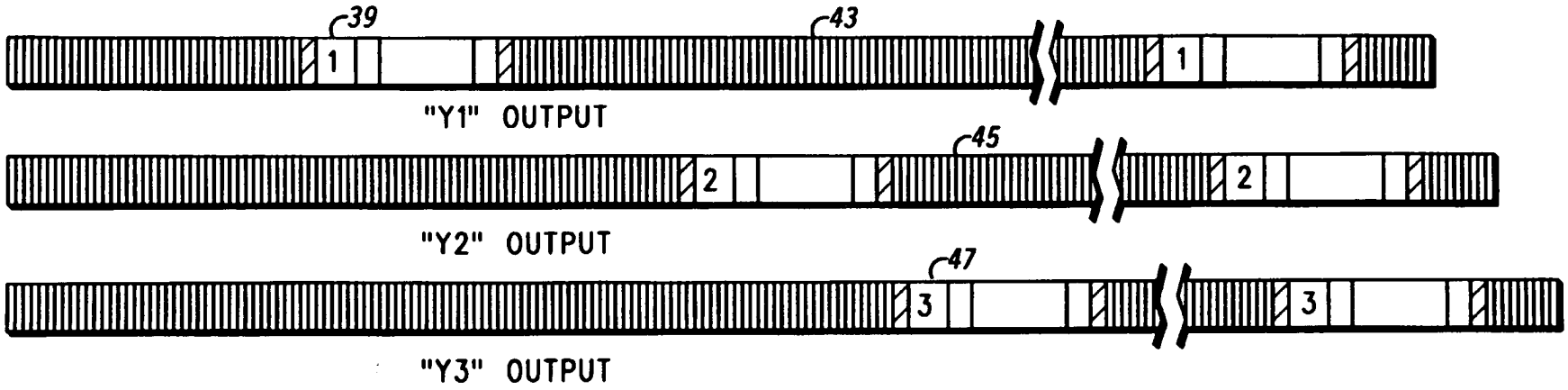


FIG. 4

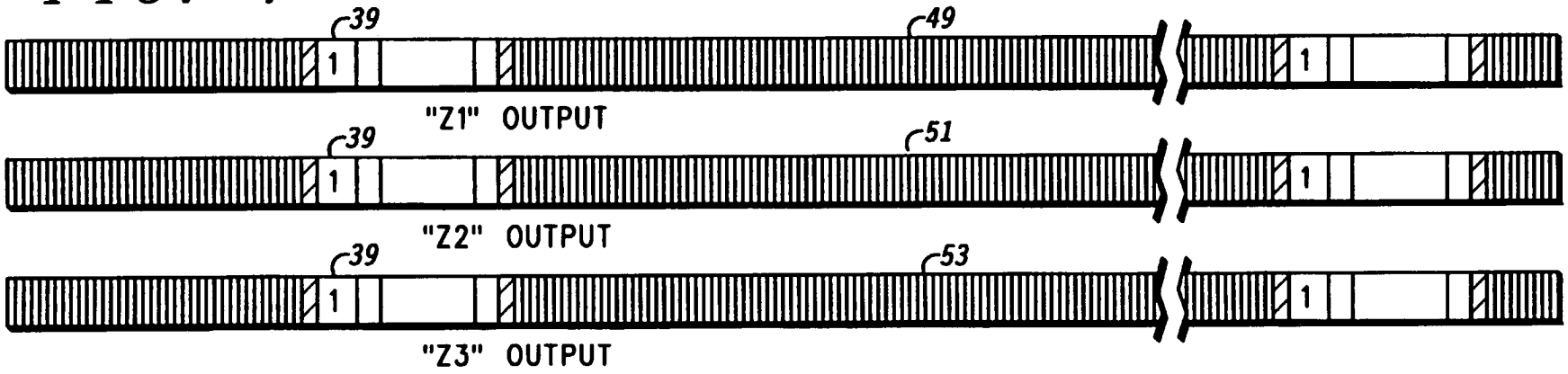


FIG. 5

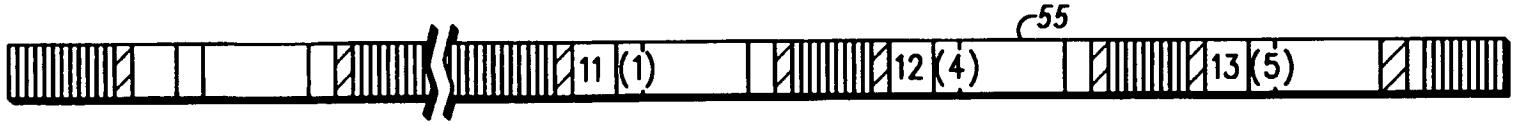


FIG. 6

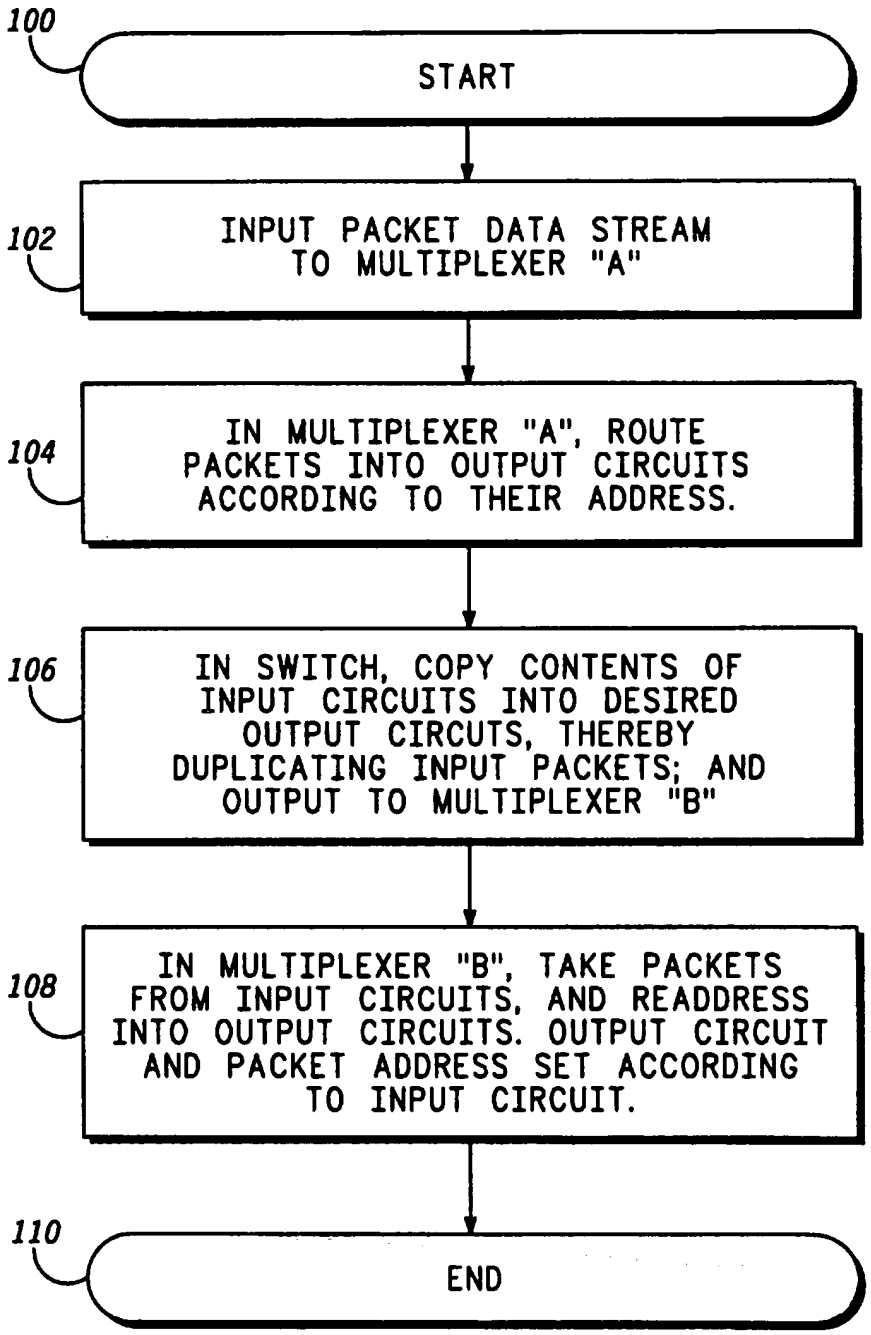

100
START
102
INPUT PACKET DATA STREAM TO MULTIPLEXER "A"
104
IN MULTIPLEXER "A", ROUTE PACKETS INTO OUTPUT CIRCUITS ACCORDING TO THEIR ADDRESS.
106
IN SWITCH, COPY CONTENTS OF INPUT CIRCUITS INTO DESIRED OUTPUT CIRCUTS, THEREBY DUPLICATING INPUT PACKETS; AND OUTPUT TO MULTIPLEXER "B"
108
IN MULTIPLEXER "B", TAKE PACKETS FROM INPUT CIRCUITS, AND READDRESS INTO OUTPUT CIRCUITS. OUTPUT CIRCUIT AND PACKET ADDRESS SET ACCORDING TO INPUT CIRCUIT.
110
END

FIG. 7

PACKET SWITCHING ARRANGEMENT AND METHOD FOR DUPLICATING INFORMATION

Field of the Invention

This invention relates to communications systems and, in particular, to packet switched data communications systems. The invention is applicable to, but not limited to, circuit switched communications systems operating in a packet switched mode.

Background of the Invention

In a multicast communications environment which employs packet switching techniques, packets of information such as voice, data and image are transmitted from a single source to multiple destinations. Such a transmission of information packets typically has three problems. First, there is an inherent delay involved, as the transmission of the same packet a number of times delays the final packet transmission by a time equal to the transmission time of the packet multiplied by the number of replications, plus any associated processing delays. Secondly, there may be a limit to the number of times a packet may be duplicated, either for timing constraints of the communications system, or for other reasons such as restrictions on processing power or memory of the duplication device. Thirdly, the packet duplicator needs to know the addresses of all destinations of the duplicated packets.

An alternative is to use a true "multicast" address approach. However, this has the disadvantage of all information packets being transmitted to all parts of the communications network, thereby unnecessarily using bandwidth.

Both of these approaches are disadvantageous when compared to the use of standard packet switching techniques known to those skilled in the art.

Thus, it is desirable to have a communications system and method of operation that seeks to mitigate some of the aforementioned problems associated with the transmission of information packets from a single source to multiple sources.

Summary of the Invention

In a first aspect of the present invention, a method for duplicating an information packet in a communications system is provided by utilising circuit switching techniques. The communications system has a circuit switch operably coupled via a plurality of communications channels to a plurality of multiplexer units. The method comprises the steps of receiving an information packet at a first multiplexer unit, wherein the information packet includes address information and information bits to be transmitted to at least second and third multiplexer units. The address information is elicited from the information packet at the first multiplexer unit and a communications channel selected for transmission of the information packet dependent upon the elicited address information. The information packet is transmitted from the first multiplexer unit to the circuit switch on the selected communications channel and the information packet duplicated at the circuit switch to provide at least two information packets for transmission on at least two outputs of the circuit switch. The at least two information packets are transmitted from the circuit switch to the at least second and third multiplexer units respectively on the at least two outputs.

Preferably, the circuit switch has timeslots for transmitting and receiving information packets, and step of duplicating the information packet at the circuit switch includes the step of duplicating the information packet in different timeslots in the at least two outputs of the circuit switch. In addition, the configuration of the circuit switch is controlled to route the information packet to the at least two outputs of the circuit switch according to the chosen communications channel input. In the preferred embodiment of the invention the address information includes a source address of the first multiplexer unit or a destination address for the information packet.

In this manner, information packets containing address information, are transmitted from a single source, the address information is elicited and the information packets duplicated. The information packets are then transmitted to multiple sources dependent upon the address information. Advantageously, there is no delay associated with multiple transmissions of the original information packet and there is no unnecessary waste of available frequency or time resource with transmitting the information packet to all areas of a communications network.

Preferably, the step of duplicating the information packet at the circuit switch further includes the step of modifying address information in the

information packet at the circuit switch thereby providing source and/or destination address information in the information packet for further routing operations of the information packet. When the address information is source address information, the step of modifying the information packet at the circuit switch includes either appending destination address information to the information packet at the circuit switch, providing source and destination address information in the information packet, or includes removing the source address information and inserting destination address information in the information packet.

In this manner, a reduced amount of address information needs to be transmitted resulting in a more efficient use of the transmitted signal.

In a second aspect of the present invention, a packet switching arrangement is provided. The packet switching arrangement comprises a first multiplexer having a first input for receiving information packets, wherein at least one information packet has address information, and a plurality of first outputs for simultaneously outputting data packets such that each information packet is transmitted to at least one of the plurality of first outputs dependent upon the address information. The packet switching arrangement further includes a circuit switch having a plurality of second inputs operably coupled to the first outputs of the first multiplexer for receiving the information packets and a plurality of second outputs for re-transmitting the information packets. In addition, the packet switching arrangement includes a second multiplexer having a plurality of third inputs operably coupled to the plurality of second outputs of the circuit switch for receiving the re-transmitted information packets, a packet address modifier for modifying the address of a packet, according to at least one of the following: the input through which it is received or the address information contained in the information packet, a combining circuit for combining modified information packets, received from the plurality of third inputs, into an output stream of information packets, an output operably coupled to the combining circuit for outputting the stream of information packets.

In this manner, the circuit switch provides a selective packet switching operation, thereby resulting in a more efficient use of the transmission bandwidth.

Preferably, the packet switching arrangement further comprises a controller for controlling the switching operation of the packet switch, thereby controlling duplication and addressing of information packets.

A preferred embodiment of the invention will now be described, by way of example only, with reference to the drawings.

Brief Description of the Drawings

FIG. 1 is a representation of an information packet, according to a preferred embodiment of the invention.

FIG. 2 is a block diagram of a packet switching arrangement, according to the preferred embodiment of the invention.

FIG. 3 is a representation of multiple information packets with different addresses, according to the preferred embodiment of the invention.

FIG. 4 is a representation of multiple information packets input to a circuit switch, according to the preferred embodiment of the invention.

FIG. 5 is a representation of multiple information packets output from the circuit switch, according to the preferred embodiment of the invention.

FIG. 6 is a representation of multiple output packets, contained in a single output circuit according to the preferred embodiment of the invention.

FIG. 7 is a flow chart showing the duplication of information packets according to the preferred embodiment of the invention.

Detailed Description of the Drawings

Referring first to FIG. 1, a representation of a single data stream, according to a preferred embodiment of the invention, is shown. The data stream is shown in a time divided structure and includes an information packet 10. The data stream consists of preamble of idle characters or flags 14, the information packet 10 and a postamble of idle characters or flags 26. The information packet 10 includes a start character 16, a header 29 containing at least one address 18, a payload 20, an optional check sequence 22, and an end character 24.

The at least one address 18, is either a source address information and/ or destination address information. The payload 20 is the information being carried in the packet, and the check sequence 22 performs a mathematical check of the integrity of the packet.

Referring now to FIG. 2, a block diagram of a packet switching arrangement, according to the preferred embodiment of the invention, is shown. The packet switching arrangement includes a first multiplexer 40, e.g. multiplexer 'A', having a first input 38 for receiving information packets,

wherein at least one information packet 10 has address information. The first multiplexer 40 has a plurality of first multiplexer outputs 42 for simultaneously outputting data packets to a circuit switch 44 such that each received information packet 10 is transmitted to at least one of the plurality of first multiplexer outputs 42 dependent upon the address information. The circuit switch 44 has a plurality of second inputs 46 operably coupled to the first multiplexer outputs 42 of the first multiplexer 40 for receiving the information packets and a plurality of second outputs 48 for re-transmitting the information packets. The packet switching arrangement includes a second multiplexer 50, e.g. multiplexer 'B', having a plurality of third inputs 52 operably coupled to the plurality of second outputs 48 of the circuit switch 44 for receiving re-transmitted information packets. The second multiplexer 50 includes a packet address modifier 54 for modifying an address of an information packet, according to at least one of the following: an input from the plurality of third inputs 52 through which it is received or address information contained in the information packet 10. The second multiplexer 50 further includes a combining circuit 56 for combining modified information packets, received from the plurality of third inputs 52, into an output stream of information packets, and an output 58 operably coupled to the combining circuit 56 for outputting the stream of information packets. In a preferred embodiment of the present invention the packet switch arrangement further includes a controller 60 having a control output 66 port for controlling the switching operation of the packet switch, thereby controlling duplication and addressing of information packets from/to first multiplexer outputs 42, second multiplexer 50 and other multiplexers 62 by control of the switching and routing of the circuit switch 44, e.g. circuit mode time division multiplex (TDM) switch.

In the preferred embodiment the circuit switch 44 is a digital switch for use in a mobile radio environment, e.g. the Ambassador Electronics Bank used on the Motorola Smartzone (Trade Mark) system. The circuit switch 44 is arranged to operate on a time division multiplexed (TDM) bus structure and is designed to take pulse coded modulation (PCM) audio signals from timeslots on incoming TDM busses, duplicate the data bytes of the PCM audio signals to particular second outputs 48 of the circuit switch 44 under the command of a controller 60, e.g. a Zone Controller. In the design of the packet switching arrangement provided in FIG. 2, the number of destination audio paths is limited by two factors: first, the number of timeslots on each TDM bus, and secondly, the number of busses present in the circuit switch

44. The maximum delay of signals being transmitted through the communications system is governed by the repeat time of timeslots on a TDM bus, and is typically fractions of a millisecond.

The multiplexers shown in FIG. 2 are responsible for managing packet to circuit address conversion and the inputs/outputs are interchangeable as shown by the arrows. In operation, multiplexer 'A' receives packets containing different information packets each with different source addresses indicating the origin of the packet, and/ or destination addresses indicating the information packet's intended destination. Based on the address information, multiplexer 'A' routes the information packets to different circuits in the TDM switch. Preferably each packet address is routed into a unique circuit such that each input circuit to the TDM switch only contains packets having a single address. In the preferred embodiment of the present invention the addressing of the packets is left unchanged at this point. Alternatively at the output of the switch, multiplex B modifies the addressing information such that the circuit number input to multiplex B signifies the output address of the packet.

A number of operational modes are available with this type of packet switching arrangement. A first mode of operation is that multiplexer 'A' operates with either source or destination based addressing. The options available at multiplexer 'A' include changing packet addresses, adding destination address information to source address information or leaving the address information unmodified. Similarly, multiplexer 'B' may change either the source or destination address of the packet to signify the destination.

A further mode of operation applies when the input packet link contains only source address information, i.e. Multiplexer 'A' routes according to source address, with multiplexer 'B' appending the destination address. Thus the output packet contains both a source and destination address, and may be further routed by other transport mechanisms (e.g. packet based networks).

Alternatively, this packet switching arrangement could operate on a single address only basis, used to signify the source address at the input, and changed by multiplexer 'B' to indicate the destination address at the output. This has the advantage of reducing packet size to the extent of one address, making the system slightly more bandwidth efficient.

FIG's 3-5 show an example of the timing structure for an information packet 10 according to a preferred embodiment of the invention. FIG. 3

shows an input data stream 41 being received at the first input 38 by multiplexer 'A'; the input data stream 41 having a first information packet 39. The multiplexer 'A' duplicates the input data stream into output busses according to the address information contained within the data stream 41. FIG. 4 shows the timing diagram of three of the plurality of first outputs 42 of the multiplexer 'A'. The three data stream outputs "y1" 43, "y2" 45, and "y3" 47 of multiplexer 'A' are shown in FIG. 4. The three outputs are simultaneously output to the circuit switch 44; the first data stream output, "y1" 43, from multiplexer 'A' containing the first information packet 39. The circuit switch 44 routes the three data stream outputs of multiplexer 'A' to three corresponding data stream outputs of the circuit switch 44; namely "z1" 49, "z2" 51, and "z3" 53, as shown in FIG. 5. Thus the packet has been duplicated onto three different output circuits, which are subsequently input to further multiplexers. FIG. 6 shows a representation of multiple output packets, contained in a single output data stream 55 from one such multiplexer. The address information of the packet, in this example, is not used after multiplexer 'A'; the address information could be removed within multiplexer 'A' such that only the payload is routed through the switch to multiplexer 'B'.

Advantageously, the use of existing PCM (pulse code modulation) switches based on TDM (time division multiplex) bus structures provides an alternative means of packet duplication. This provides advantages in both speed and duplication abilities.

If packets of data, intended for multicasting, are incorporated into incoming PCM streams, for example by multiplexer 'A' separating data packets into particular different circuits by eliciting destination address information, the circuit switch 44 simply needs to be configured as it would be for circuit mode PCM speech. Packets of data contained within input streams are advantageously duplicated across the required number of output streams with virtually no delay. At the output of the device, further multiplexers combine the outputs back into multiple packets per link, to return to a low-link bandwidth format.

Referring now to FIG. 7, a flowchart of the timing of communications within the communications system, in accordance with a preferred embodiment of the invention, is shown. The method for duplicating information in a communications system, having a circuit switch operably coupled via a plurality of communications channels to a plurality of multiplexer units, includes the steps of receiving an information packet at a

first multiplexer unit, e.g. multiplexer 'A', as shown in step 102, wherein the information packet includes address information and information bits to be transmitted to at least second and third multiplexer units. The address information is elicited from the information packet at the first multiplexer unit and a communications channel selected for transmission of the information packet dependent upon the elicited address information, as shown in step 104. The information packet is transmitted from the first multiplexer unit to the circuit switch on the selected communications channel and duplicated at the circuit switch to provide at least two information packets for transmission on at least two outputs of the circuit switch, as shown in step 106. The at least two information packets are transmitted from the circuit switch to the at least second and third multiplexer units respectively on the at least two outputs.

Preferably, information packets are re-addressed at the at least second and third multiplexer units and transmitted from the respective multiplexer as a single data stream, as shown in step 108.

In a preferred embodiment of the invention the communications system has timeslots for transmitting and receiving information packets, and the step of duplicating the information packet at the circuit switch to provide at least two information packets for transmission on at least two outputs of the circuit switch, includes the step of duplicating the information packet in different timeslots in the at least two outputs of the circuit switch. In addition, the step of duplicating the information packet further includes the step of controlling the configuration of the circuit switch to route the information packet to the at least two outputs of the circuit switch according to the chosen communications channel input. When the address information is source address information, the step of modifying the information packet at the circuit switch includes either: (i) appending destination address information to the information packet at the circuit switch providing source and destination address information in the information packet for further routing operations of the information packet, or (ii) removing the source address information and inserting destination address information in the information packet at the circuit switch for further routing operations of the information packet.

Thus, a packet switching arrangement is provided that seeks to mitigate some of the aforementioned problems associated with the transmission of information packets from a single source to multiple sources.

In addition a method of operation shows a preferred method of achieving a duplication and re-transmission of such information packets.

Claims

1. A method for duplicating an information packet in a communications system having a circuit switch operably coupled via a plurality of communications channels to a plurality of multiplexer units, the method comprising the steps of:

receiving an information packet at a first multiplexer unit, wherein the information packet includes address information and information bits to be transmitted to at least second and third multiplexer units;

eliciting the address information from the information packet at the first multiplexer unit;

selecting a communications channel for transmission of the information packet dependent upon the elicited address information;

transmitting the information packet from the first multiplexer unit to the circuit switch on the selected communications channel;

duplicating the information packet at the circuit switch to provide at least two information packets for transmission on at least two outputs of the circuit switch; and

transmitting the at least two information packets from the circuit switch to the at least second and third multiplexer units respectively on the at least two outputs.

2. The method according to claim 1, wherein the step of duplicating the information packet further includes the step of controlling a configuration of the circuit switch to route the information packet to the at least two outputs of the circuit switch according to the chosen communications channel input.

3. The method according to any of the preceding claims, wherein address information includes at least one of the following: a source address of the first multiplexer unit, a destination address for the information packet.

4. The method according to any of the preceding claims, wherein the communications system has timeslots for transmitting and receiving information packets, and the step of duplicating the information packet at the circuit switch to provide at least two information packets for transmission on at least two outputs of the circuit switch includes the step of duplicating the information packet in different timeslots in the at least two outputs of the circuit switch.

5. The method according to any of the preceding claims, wherein the step of duplicating the information packet at the circuit switch further includes the step of modifying address information in the information packet at the circuit switch providing source and/or destination address information in the information packet for further routing operations of the information packet.

6. The method according to claim 5, wherein the address information is source address information and the step of modifying the information packet at the circuit switch includes appending destination address information to the information packet at the circuit switch providing source and destination address information in the information packet for further routing operations of the information packet.

7. The method according to claim 5, wherein the address information is source address information and the step of modifying the information packet at the circuit switch includes removing the source address information and inserting destination address information in the information packet at the circuit switch for further routing operations of the information packet.

8. A packet switching arrangement comprising:

a first multiplexer having

a first input for receiving information packets, wherein at least one information packet has address information, and

a plurality of first outputs for simultaneously outputting data packets such that each information packet is transmitted to at least one of the plurality of first outputs dependent upon the address information;

a circuit switch having a plurality of second inputs operably coupled to the first outputs of the first multiplexer for receiving information packets and a plurality of second outputs for re-transmitting information packets; and

a second multiplexer having

a plurality of third inputs operably coupled to the plurality of second outputs of the circuit switch for receiving re-transmitted information packets,

a packet address modifier for modifying an address of an information packet, according to at least one of the following: an input through which the information packet is received, address information contained in the information packet,

a combining circuit for combining modified information packets, received from the plurality of third inputs, into an output stream of information packets, and

an output operably coupled to the combining circuit for outputting the stream of information packets.

9. The packet switching arrangement of claim 8, further comprising a controller for controlling a switching operation of the circuit switch, thereby controlling duplication and addressing of information packets.

The Patent Office

13

Application No: GB 9602292.6
Claims searched: 1-9

Examiner: Simon Rees
Date of search: 8 May 1996

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.O): H4K (KTK, KTS), H4P (PPS)

Int Cl (Ed.6): H04L (12/56, 12/52, 12/18), H04J (3/26), H04Q (11/04)

Other: Online: WPI, INSPEC

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
A	GB2273224A	(NETCOMM) Whole document, especially lines 5-14 of page 4 and lines 10-20 of page 12.	1, 8.
A	GB2238934A	(ADAPTIVE CORP) Whole document, especially the last two lines on page 1 to line 19 of page 2.	1, 8.
A	WO94/24794A1	(WASHINGTON UNIVERSITY) Whole document, especially from line 21 of page 2 to line 5 of page 3, and lines 16-24 of page 9.	1, 8.

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.